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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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22150	7590	07/18/2006		EXAMINER
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			GEORGE, PATRICIA ANN	
			ART UNIT	PAPER NUMBER
			1765	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,931	PARK ET AL.	
	Examiner Patricia A. George	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 18 May 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 33 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/9/05.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3, 13-14, 21, 23 and 28-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "in a direction of" in claims 1-3, 13-14, 21, 23 and 28-29 is a relative term which renders the claim indefinite. The term "in a direction of" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "in the direction of" fails to illustrate the intended position of the claimed element. The instant invention is a three dimensional object, which would have several descriptive directional references that could be used. Please modify the claimed language to be more specific than "in the direction of". All claims either directly or indirectly dependent on the above claims are rejected as being indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-4, 6-12, 15-18, 21-27, 30 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Hayano et al. of USPN 6,403,413.

As for claims 1 and 21, Hayano et al. discloses a method for manufacturing a semiconductor device (c.1, l.16): forming word lines (fig.37, p.WL(5)-written on gate electrodes) on a DRAM substrate (col.13, l.3-5); forming a first insulating layer for penetration holes that connect to the plurality of gate regions including both n and p-types. See col.2, l.20-22, or fig.37, part 5 for the gate line. Note part 9 as the 1st insulator; note part 11b as the contact to the gate lines (written on contact pads). Part 11b is wiring in a contact hole that is used to make contact with the gate (col.2, l. 23-24 – written on contact pads). A second contact, is disclosed, that connects the n-type region for the data lines (fig.36, DL). Both sets of contacts are electrically connected to the semiconductor substrate (see figures 36 and 37). Hayano also discloses forming a second insulating layer (part 12 in fig. 36-37) to cover the first contact pads and the second contact pads (col.2, l. 25). Hayano discloses forming data lines in figure 36, part DL, which is written on bit lines. Hayano discloses the bit lines (DL) cross over the gate lines (WL) in figure 25. Note part DL runs on the Y axis and part WL runs on the X axis. In figure 36, Hayano discloses the bit lines (DL) are electrically connected to the second contact pads (11a) by penetrating the second insulating layer (12) via parts 13 and 14. In figure 36, Hayano discloses forming a third insulating layer (15/16) to

cover the bit lines (DL). Hayano discloses after the 3rd insulative film (fig.37, 15/16) is deposited, through holes are formed such that a portion of the plug (written on contact pad, part. 11b) is exposed (see fig.26, hole 17 and col.16, l.1-7). Hayano discloses the hole is formed by use of a hard mask (fig. 27, 18 or col.16, l.19) which is written on selectively etching. Hayano discloses the 3rd insulating layer (fig. 37, 15/16) wherein the opening crosses the bit lines (line pattern defined in embodiment #24) and exposes the first contact pads (fig. 37; 11b). Hayano discloses forming a polysilicon plug (figure 29-31, part 19) in each through hole (figure 29-31,p. 17) and further a barrier metal film (figure 29-31, p. 20) is formed on a surface of each plug (figure 29-31, p.19). An n-type polycrystalline silicon film doped with phosphorus (P) is deposited on the insulative film (figure 29-31, part 16) by CVD method, which embeds the polysilicon inside each through hole (figure 29-31, part 17). The n-type polycrystalline silicon film deposited outside of each through hole is removed by chemical mechanical polishing (CMP) method or etch back. And, at this time, the n-type polycrystalline silicon film deposited in each through hole 17 is over-polished (over-etched) to retreat the surface of each plug (figure 29-31, part 19) downward from a surface of the insulative film (figure 29-31, part 16). Each space for embedding the barrier metal film (figure 29-31, part 20) is secured in an upper portion (written on patterned) of each plug 19. Next, by depositing a TiN film by sputtering, the TiN film is embedded into each through hole on the upper portion of each plug. Thereafter, the TiN film deposited outside each through hole 17 is removed by CMP or etch back. Hayano discloses other types of barrier metal may be used such as: ruthenium (Ru) polycide, titanium (Ti)-aluminum(Al)-silicon (Si) alloy

or the like can be used in addition to TiN. Hayano discloses the contact between both holes (col.16, 56-57) whichis written on being electrically connected to first contact pad. Hayano discloses the contact through hole (figure 29-31, part 17) and the bit lines (part DL) face each other (col.16, l.64-66 is written on in the direction of the bit line). Hayano discloses forming a lower electrode of the storage capacity element (fig. 37, p. 24) in the insulative film (col.17, 39-42 or fig. 32-33, part 21) is made of CVD TEOS flattened by CMP (col.17, l.48-52). Hayano discloses the information storage capacity element (fig. 37, p. 24) includes a lower electrode (fig. 37, p.24a), a capacity insulative film (fig. 37, p.24b), and a plate electrode (fig. 37, p.24c). Hayano discloses the lower electrode (fig. 37, 24a) is formed, for example, of a doped polysilicon film, and is electrically connected to one end of each n-type semiconductor region (fig. 37, p.7) of one of a source/drain of the memory cell selecting MISQs through the plugs (fig. 37, p.19) and plugs (fig. 37, 11b) formed in a lower layer thereof (col.18, l.19-27).

As for claims 2 and 22, see figure 37, for Hayano's discloser of the first contacts (part 11b), arranged between the word lines (WL) in multiple columns, that are defined by sequential word lines.

As for claims 3 and 23, see figure 34, where Hayano discloses the word lines are band-type and in the y direction, also see figure 57A where Hayano discloses other band-type lines extend in the y direction, same direction as said word lines, which is written on gate lines. (also note text references Embodiment 24, and col. 13, l.21-22).

As for claims 4, see figure 15 where Hayano discloses parts 11b, which are band-type openings formed to expose the first contact pads. Hayano discloses

surrounding by parts 9 which are the first insulation layers between the part WL, which are word lines that are written on gate lines.

As for claims 6 and 26, Hayano discloses in Figure 27, part 12 which fills a band type opening which has a width that remain on portions of two gate lines that are adjacent. See figure 25 where Hayano discloses the configuration of data line in relation to word line and electrode therefor.

As for claim 7, see figure 26, where Hayano discloses forming band-type openings represented by part 17, which are formed by using part 18, a photoresist hardmask, which sits on part 15, the third insulating layer, that is used to selectively etch the banded pattern of part 17. In figure 27, Hayano discloses part 15, prior to patterning, cover the first contact pads, but was subsequently patterned in figure 28 to expose portions of parts 12 and 15, the second and third insulating layer. Hayano teaches, in column 16, lines 18-20 "each hard mask 18 is formed by using each photoresist pattern as an etching mask". Hardmask is written on insulative material.

As for claim 8, see figure 28 where Hayano discloses parts 18 and 18a which function as cap and spacer to provide cover and sidewall protection for part DL, the data lines (written on bit lines), during the etching of part 17, a contact space, which is written on a capping and sidewall insulative layer that prevents damage to the bit lines.

As for claim 9, see Figure 28 where Hanyo discloses patterning of part 17, the opening for the next conductive layer, is carried out by using parts 18 and 18a, a cap and sidewalls, as the hardmask, which is written on an etch stopper (col. 16, l. 38-39).

As for claim 10, see above where the polysilicon layer is written on in detail (claim 1).

As for claim 11, Hayano discloses use of reflection preventing film and photo-resist layers (col.17, l.36) with optional use of a hardmask (col.17, l.66-67) to form part 22 of figures 32-32, the capacitor hole, on part 21, an insulative film, which can be CVD TEOS (col.17, l.48-49), which is then plasma etched (col.18, l.5-7) to expose the barrier metal at the bottom of the hole (col.18, l.8-9), which is written on partially exposing portions of the conductive layer overlapping the bit lines and portions of the conductive layer overlapping the second contact pads disposed between the gate lines and etching the exposed portions of the conductive layer by using a second photo-resist pattern as an etch mask.

As for claims 12 and 27, Hayano discloses the direction of the data and word lines in column 18, lines 9-12, which is written on extensions of two adjacent storage electrode contact bodies, between which the bit line is disposed, extend in opposite direction from each other. Also see figure 34 for line configurations.

As for claims 15, and 16 see figure 34 where Hayano discloses part DL, the bit line, is disposed between two part 17s that form part 5, adjacent storage electrodes, which are positioned at an angle to part DL, the bit line, and part WL, the gate line. This discloser is written on claims 15 and 16.

As for claims 17, 18, 30, and 31 Hayano discloses the shape of holes in Embodiment 23. Hole pattern: this means a fine pattern such as a contact hole and a through hole having two dimensional size equal to or smaller than exposure

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wavelength on a wafer. In generally, shape thereof is square, or rectangle close to the square, or octagon on a mask, or the like, but is circular on the wafer in many cases. Hayano's discloser is written on the shapes: cylindrical, circular, elliptical, or rectangular area as in claims 17 and 18.

As for claims 24, see figure 15 where Hayano discloses parts 11b, which are band-type openings formed to expose the first contact pads. Hayano discloses surrounding by parts 9 which are the first insulation layers between the part WL, which are word lines that are written on gate lines.

As for claims 25, see figures 36 and 37, where Hayano illustrates parts 23 and 24 are formed in banded openings, and the perspective widths, are greater than width of part 11b.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5, 13, 14, 28 and 29 are rejected under 35 U.S.C. 103(a) as being obvious over Hayano (see discussion above) USPN 6,403,413, in view of Takeda et al. of US 2001/0045589.

Hayano does not disclose the width of the band-type opening is greater than the width of the first contact pad, poly electrode is wider than gate electrode under it, as in claim 5. Hayano does not disclose the poly electrode has an extensions that is wider than the main body, as in claim 13. Hayano does not disclose the extensions of the poly electrode have unequal side widths, the extension on the bit line side being of greater width than the extension on the gate line side, as in claim 14. Hayano does not disclose the electrode supporting layer includes an etch stop layer that is used as an etch stopper when the mold is removed, as in claims 20 and 33.

As for claims 5, see figures 36 and 37, where Hayano illustrates parts 23 and 24 are formed in banded openings.

It is noted that the reference of Hayano is silent about the width of the band-type opening is greater than a width of the first contact pad. However, such a dimension does not distinguish over the teaching of the width of the band-type opening is greater than a width of the first contact pad.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select the width of the band-type opening is greater than a width of the first contact pad, including the specific dimensions in applicants claim 5, because it has been held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device

having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. See MPEP 2144.04 charges in size/proportion and In re Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984).

It is also noted that the reference of Hayano fails to disclose the specific structural proportions defined in claims 13, 14, 28, and 29.

However, It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select the proportion of components including those defined in applicants' claims 13, 14, 28, and 29 because it has been held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. See MPEP 2144.04 charges in size/proportion and In re Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984).

Claim Rejections - 35 USC § 103

Claims 19, 20, 32 and 33 are rejected under 35 U.S.C. 103(a) as being obvious over Hayano (see discussion above) USPN 6,403,413, in view of Goebel et al. of US 2001/0041406.

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As for claims 19 and 32, in figure 37, Hayano discloses part 20, which illustrates supporting part 23, the electrode. Hayano's part 16 covers part 19, which is a contact body. Hayano also forms part 21, on part 20, the electrode supporting layer. See figure 36, for illustration of the patterning of part 21, which is written on the mold layer. Hayano's part 23, the storage electrode, is formed in the banded spaces of part 21, which form the shape of the storage electrode, and is written on forming a conductive layer on the mold. The result is shown in figure 37, where the banded pattern of the conductive layer is clearly separated into individual storage electrodes.

Hayano does not disclose the removal of the electrode mold, as in claims 19 and 32. Hayano does not disclose the the electrode supporting layer includes an etch stop layer that is used as an etch stopper when the mold is removed, as in claims 20 and 33.

Goebel et al. teaches a method for molding electrodes in microelectronic devices. (para. 0010, l.1) Goebel teaches the removal of the filler material, with is written on the electrode mold in paragraph 0017, as in claims 19 and 32. Goebel teaches the plasma etching is used to remove the material (para. 0042), which is written on the electrode supporting layer including an etch stop layer when the mold is removed, as in claims 20 and 33.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the method of molding electrodes, of Goebel, in the

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DRAM process, of Hayano, because Goebel teaches use of the technique of molding electrodes makes it possible to increase the achievable capacitance, which is directly proportional to the electrode area, particularly in stacked capacitors of DRAM devices, resulting in decreased manufacturing cost.

Response to Arguments

Applicants argue that the embodiment descriptions and figures in the specification, with and skill in the art, would able one to understand to scope of the term “in the direction of” as recited in claims 1-2, 13-14, 23, and 28-29.

Examiner disagree, as stated in the 35 US 112 rejection above: The term “in the direction of” fails to illustrate the intended position of the claimed element. The instant invention is a three dimensional object, which would have several descriptive directional references that could be use. Please modify the claimed language to be more specific than “in the direction of”.

Applicants argue, on page 12, that Hayano fails to teach selectively etching a third insulating layer to form a band type opening, wherein the band type opening crosses the bit lines and exposes the first contact pads.

Examiner disagrees as Hayano discloses part 15/16 of figure 37, is deposited then has holes formed in it, which is written on selective etching (see fig.26, hole 17 and col.16, l.1-7). As for, “to form a band type opening” Hayano discloses forming band-type openings represented by part 17, which are formed by using part 18, a photoresist hardmask, which sits on part 15, the third insulating layer, that is used to selectively

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etch the banded pattern of part 17. Hayano discloses the 3rd insulating layer (fig. 37, 15/16) wherein the opening crosses the bit lines (line pattern defined in embodiment #24) and exposes the first contact pads (fig. 37; 11b).

Applicants argue, on page 12, that hayano fails to teach each of the contact bodies include an extension that is extended on the third insulating layer.

Examiner disagrees as Hayano teaches a hole is formed by use of a hard mask (fig. 27, 18 or col.16, l.19) to form openings in the 3rd insulating layer (fig. 37, 15/16) wherein the opening crosses the bit lines (line pattern defined in embodiment #24) and exposes the first contact pads (fig. 37; 11b) to form a polysilicon plug (figure 29-31, part 19) in each through hole (figure 29-31,p. 17) and further a barrier metal film (figure 29-31, p. 20) is formed on a surface of each plug (figure 29-31, p.19). This teaching by Hayano is very clear about the plug being formed of one material, then having another material formed on top of it (i.e. extension) being in contact with (i.e. "on") the third insulating layer. Examiner interprets extension the condition of being extended (see dictionary.com) and finds any part that is a means to extend some other part, an extension.

Applicants argue, on page 13, that Hayano's contact holes do not cross bit lines.

Please see paragraph above that references Hayano opening crossing bit lines.

As to applicant's argument, on page 13, that Hayano's contant holes are clearly not band-type openings, examiner disagrees.

Examiner interprets band-type openings to mean a strip or stripe that contrasts with something else in color, texture, or material (see dictionary.com "banded").

Further, the claim language provides no negative language that would exclude contact holes.

All responses to arguments presented above, may be found in the rejection above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is: USPN 5817562 claims hard mask materials made of insulators, as does SN 09/920927, SN 09/225887 and SN 09/847,289 all illustrate electrode extensions wider than main body; SN 09/847289 also teaches the electrode base is wider than the contact pad.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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06/06

Patricia A George
Examiner
Art Unit 1765

NADINE NORTON
SUPERVISORY PATENT EXAMINER
ART UNIT 1765

